Design of Fully-Integrated RF Front-End Receiver for Large Image Rejection

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• Front-End Receiver Architecture
• Building Blocks Design
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• Conclusion
Introduction

- Evolution of the wireless communications
  - Growth of standards, customer needs
  - Design of complex electronic devices:
    - Multi-standards
    - Multi-functions (voice, internet, GPS, etc.)

- Efforts on IC design & implementation
  - Constraints:
    - High integration, low-cost, low-power
  - Challenges in analog part of RF transceivers:
    - Process high frequency signals
    - Choose the scaled technology (CMOS)
Front-End Architecture

- Double quadrature front-end receiver architecture
  - Better image rejection performance (*comparing to the low-IF one*)
  - Including circuits for magnitude matching balance

```
RF tunable PPF

Switch mixers

IF PPF

Buffer

OTA

IF1

I

RF

x4

Frequency control

LOQ

Q

LO1

Quadrature LO

differential path
```
Building Blocks Design

- **Polyphase Filters** (used in RF & IF sections)
  - Accurate I/Q signals generation
  - High Image Rejection Ratio (IRR)
Building Blocks Design

- **Image rejection problem**

- **Solution: Image reject Filter (Polyphase filters)**
Polyphase Filter

Principle

• Pole frequency (notch) :

\[ f_p = \frac{1}{2\pi RC} \]
### Design constraints

- **Process tolerance & Components mismatch**
  - Components with large surface: decrease the mismatch, but increase the parasitics.
  - Tradeoff among chip area, IRR and freq.
  - Statistical study of the IRR distribution
  - **Choice**: PPF with 4 stages (RF & IF)

- **Careful attention to layout matching**
  - Optimal sizing (components & connexions)
  - Conserve the circuit symmetry
  - Balance the I/Q paths parasitics
  - Characterize the interconnexion network
Polyphase Filter

- **Tuning feature**
  - RC basic passive polyphase network + MOS resistors
  - Frequency control (by tuning $V_G$): $f_p = \frac{1 + RK \frac{W}{L} (V_G - V_T)}{2\pi RC}$
  - Bandwidth centered at 2.4GHz (can be tuned by 300MHz)

![Diagram of Polyphase Filter](image)

**PLS results**

<table>
<thead>
<tr>
<th>Frequency (Hz)</th>
<th>IRR (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1E9</td>
<td>-70</td>
</tr>
<tr>
<td>2E9</td>
<td>-65</td>
</tr>
<tr>
<td>3E9</td>
<td>-60</td>
</tr>
<tr>
<td>4E9</td>
<td>-55</td>
</tr>
<tr>
<td>5E9</td>
<td>-50</td>
</tr>
</tbody>
</table>

IRR $\approx$ 73dB

130nm CMOS technology

(192 x 97 µm²)

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Building Blocks Design

- **Double-Quadrature down-converter**
  - Both LO and RF inputs applied in quadrature

![Diagram of Double-Quadrature down-converter]
Double-Quadrature Mixer

- **Switch mixer**
  - Large IRR, low-power, high linearity
  - Four MOS transistors operating in the linear region ($R_{on}$)

- **OTA** (*Folded-cascode common-mode feedback*)
  - High voltage gain

- **Resistive feedback**
  - Magnitude matching depends on $R$.
  - Adjusting resistors corrects the magnitude mismatch

$$V_{IF-I+} = V_{RF-I+} \cdot \sin(\omega_{IF-I+}t) \frac{R_{2a}}{R_{1a} + R_{on}}$$
Image-Rejection Front-End Results

- Implemented in 130nm CMOS technology

Total image rejection results (with PLS scheme)

\[
\begin{array}{c|c}
\text{IF band: [5, 9]MHz} & \\
\text{IRR} & \approx 61\text{dB}
\end{array}
\]
Image-Rejection Front-End Results

- **Magnitude mismatch impact on the IRR**

- Uniform image rejection in the IF band
- Great immunity of the chain to different magnitude mismatches

\[ \Delta IRR < 2.5\text{dB around 61dB} \]  
(for \( \Delta A < 20\% \))
### Image-Rejection Front-End Results

#### Comparison with previous works

<table>
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<tbody>
<tr>
<td>CMOS Process</td>
<td>0.13µm</td>
<td>0.18µm</td>
<td>0.6µm</td>
<td>0.18µm</td>
<td>0.18µm</td>
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<tr>
<td>Supply voltage</td>
<td>2.5V</td>
<td>1.8V</td>
<td>3.3V</td>
<td>1.8V</td>
<td>1.8V</td>
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<td>RF frequency</td>
<td>2.4GHz</td>
<td>1.22GHz</td>
<td>2.4GHz</td>
<td>5.25GHz</td>
<td>2.4GHz</td>
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<td>-</td>
<td>1GHz</td>
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<tr>
<td>IRR</td>
<td><strong>61dB</strong></td>
<td>58dB</td>
<td>60dB</td>
<td>55dB</td>
<td>35dB</td>
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<tr>
<td>NF</td>
<td>25dB</td>
<td>20dB</td>
<td>7.2dB</td>
<td>7dB</td>
<td>10dB</td>
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<tr>
<td></td>
<td>(sans LNA)</td>
<td>(sans LNA)</td>
<td>(avec LNA)</td>
<td>(avec LNA)</td>
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<tr>
<td>IIP3</td>
<td><strong>14dB</strong></td>
<td>-</td>
<td>-3.4dBm</td>
<td>2.5dBm</td>
<td>-15dBm</td>
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<tr>
<td>Consumption</td>
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<td>6.11mA</td>
<td>10.6mA</td>
<td>23.33mA</td>
<td>5mA</td>
</tr>
<tr>
<td>Area</td>
<td>0.96mm²</td>
<td>1.57mm²</td>
<td>3.18mm²</td>
<td>4mm²</td>
<td>0.5mm²</td>
</tr>
</tbody>
</table>
Conclusion

- **Context**: Growth of wireless communication
- **Objective**: Increasing the IRR & the matching
- **Design of an RF front-end receiver**
  - Double-quadrature architecture
  - PPF (optimal components configuration, tunable feature)
  - Switch mixers (high linearity with structure of magnitude matching control)
- **Obtained performances (PLS)**
  - High image rejection ($\approx 61$dB)
  - High linearity
  - Good immunity to mismatch
Thank You For Your Attention

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References


