A 3 GHz DLL-Based Clock Generator with Stuck Locking Protection

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Outline

- Introduction
- Architecture
- Layout
- Simulation Results
- Performance Comparisons
- Conclusion
- References
Recently, the chip-to-chip data communication bandwidth limits the high-speed IC fabrication technology.

- The demands for data bandwidth in network has driven the development.

High-speed and serial link technologies: SATA, PCI-E, USB
CLK Gen on Tx

- DLL-based CLK Gen
  - Non-accumulation jitter

- Motivation for Proposed Architecture
  - The sensitivity of half transparent (HT)
  - Stuck locking error
  - Frequency multiplier (FM)
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**DLL Architecture**

- **MDCC**
  - Stuck locking
  - Sensitivity of HT

- **FM**
  - High Frequency Clock

![Diagram of DLL Architecture]

- Ref. Clock 250 MHz
- VCDL
- MDCC
- PD
- CP
- LPF
- Out1Out2
- Out12
- To TX Architecture
- FM
- Synthesized Clock
  - 3 GHz
PD with Half-Transparent (HT) Architecture

- **Advantages**
  - Small dead zone
  - Dynamic logic ➔ Can operate in high speed
  - Low area cost

- **Disadvantages**
  - Dynamic logic ➔ Minimum operation frequency
  - Duty sensitivity
**Locking Error**

- **Stuck locking**
  - The difference between Phase1 and Phase2 $< 0.5 \ T_{CLK}$
  - An impossible case

- **Harmonic locking**
  - The difference between Phase1 and Phase2 $> 1.5 \ T_{CLK}$
  - Lock in the Nth cycle

- **Locking range**
  - $0.5 \ T_{CLK} < T_{VCDL} < 1.5 \ T_{CLK}$
Half-Transparent (HT) Architecture Error

- If duty cycle is varied, there are two properly error cases
  - When duty is too large ➔ HT can only detect once
  - When duty is too small ➔ HT can not operate correctly
Architecture of PD with MDCC

MDCC

Phase 0° → 0
Phase 180° → 1

Phase 360° → 0
Phase 180° → 1

2 to 1 MUX

TF/F

DCC_{Out01}

Up

PD

DCC_{Out02}

Dn

CP

Ref. Clock

250MHz

VCDL
Duty Cycle Corrector (DCC)

- There are two kinds of $DCC_{Out}$
  - It would make two different results if the initial values are different.
  - The phase difference of two $DCC_{Out}$ is $180^\circ$. 
To avoid two kinds of \( \text{DCC}_{\text{Out}} \)
- Phase \( 0^\circ : 0 \rightarrow 1 \)
- Phase \( 180^\circ : 1 \rightarrow 0 \)
- By this design, there is only one kind of \( \text{DCC}_{\text{Out}} \).

Just use two phases (Compare to the original)
Operation of HT with MDCC

- **Error case**

According to MDCC, new signals $DCC_{Out1}$ and $DCC_{Out2}$ are no longer an error case.
Whether lead or lag, PD with MDCC can work correctly
PD with MDCC

- When DLL is unlocking
  - DCC\textsubscript{Out}'s duty cycle is not 50%
  - PD still can work correctly

- When DLL is locking
  - DCC\textsubscript{Out}'s duty cycle is 50%
When stuck locking occurs, PD with MDCC can still work.
- If use the original DCC, PD can not work correctly.
- If use the modified DCC, PD still can work correctly.

MUX and Flip-flop in MDCC need to be designed.
Control

- Accurate control $\Rightarrow V_{\text{ctrl}}$ dominates both NMOS and PMOS

- Multiphase outputs
Frequency Multiplier (FM)

- One Shot Circuit ➔ Pulse generation
- Symmetric AND ➔ Edge combination

One Shot

Symmetric AND

Out01
Out03
Out02
Out04
Out05
Out07
Out06
Out08
Out09
Out11
Out10
Out12

OS_01
OS_03
AND1_1
AND1_2
AND2_1
AND2_2
AND3_1
AND3_2

FM_{out}

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Frequency Multiplier (FM)

Timing diagram

- Out01
- OS_01
- Out03
- OS_03
- AND1_1
- AND1_2
- AND2_1
- AND2_2
- AND3_1
- AND3_2

Voltage (V)

Time (s)
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Chip Layout

Chip dimensions: 745 um x 745 um

Features:
- Band
- PD
- CP
- VCDL
- LFF
- FM
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Simulation Results

- Post-layout simulation (DLL @ 500 MHz)

Vctrl and Vctrl-Vss_VCDL

Jitter diagram of one phase

Multiphase

Statistics of 12 phases

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Simulation Results

- Pre-layout simulation (DLL @ 250 MHz, FM_{Out} @ 3 GHz)
  - Eye diagram of one phase
  - Jitter diagram of FM_{Out}

- Post-layout simulation (DLL @ 250 MHz, FM_{Out} @ 3 GHz)
  - Eye diagram of one phase
  - Jitter diagram of FM_{Out}
Simulation Results

- Post-layout simulation (DLL @ 250 MHz, FM\textsubscript{Out} @ 3 GHz)

![Graph showing statistics of 12 phases](image)

- Statistics of 12 phases

![Jitter diagram of FM\textsubscript{Out}](image)

- Jitter diagram of FM\textsubscript{Out}

8.31% @ 6000 hits

31.17 ps @ 6000 hits
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- **Performance Comparisons**
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## Specification

<table>
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<tr>
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<th>Pre-layout</th>
<th>Post-layout</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Process</strong></td>
<td>TSMC 180 nm</td>
<td></td>
</tr>
<tr>
<td><strong>Supply Voltage</strong></td>
<td>1.8 V</td>
<td></td>
</tr>
<tr>
<td><strong>DLL Frequency</strong></td>
<td>250 MHz</td>
<td></td>
</tr>
<tr>
<td><strong>DLL Multi-phases</strong></td>
<td>12</td>
<td></td>
</tr>
<tr>
<td><strong>FM Output Frequency</strong></td>
<td>3 GHz</td>
<td></td>
</tr>
<tr>
<td><strong>Power</strong></td>
<td>20.5 mW @ 3 GHz</td>
<td>20.9 mW @ 3 GHz</td>
</tr>
<tr>
<td><strong>DLL Jitter(p-p)</strong></td>
<td>539 fs @ 500 MHz</td>
<td>2.31 ps @ 500 MHz</td>
</tr>
<tr>
<td><strong>FM Jitter(p-p)</strong></td>
<td>22.2 ps @ 3 GHz</td>
<td>31.17 ps @ 3 GHz</td>
</tr>
<tr>
<td><strong>Chip Area</strong></td>
<td>745 um x 745 um</td>
<td></td>
</tr>
</tbody>
</table>
## Performance Comparisons

<table>
<thead>
<tr>
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</thead>
<tbody>
<tr>
<td>Process (nm)</td>
<td>180</td>
<td>130</td>
<td>180</td>
<td>130</td>
<td>180</td>
</tr>
<tr>
<td>Supply voltage (V)</td>
<td>1.5</td>
<td>1.2</td>
<td>1.8</td>
<td>1.2</td>
<td>1.8</td>
</tr>
<tr>
<td>Output (GHz)</td>
<td>0.05-0.5 (10X)</td>
<td>0.04-0.8 (20X)</td>
<td>0.04-0.5 (12.5)</td>
<td>0.015-0.6 (40X)</td>
<td>0.05-0.5 (10X)@DLL 0.6-3 (5X)@FM</td>
</tr>
<tr>
<td>Jitter (ps, p-p)</td>
<td>11.1 @ 500MHz</td>
<td>12 @ 700 MHz</td>
<td>12 @ 550 MHz</td>
<td>N.A.</td>
<td>2.94 @ 250 MHz 31.17 @3 GHz (12X)</td>
</tr>
<tr>
<td>Jitter (ps, rms)</td>
<td>1.43 @ 500MHz</td>
<td>1.6 @ 700 MHz</td>
<td>1.5 @550 MHz</td>
<td>8.9 @ 600 MHz</td>
<td>3.01 @ 600 MHz 4.01 @2.5 GHz</td>
</tr>
<tr>
<td>Power (mW)</td>
<td>6</td>
<td>43</td>
<td>12.6</td>
<td>20</td>
<td>20.9 @3 GHz</td>
</tr>
<tr>
<td>Core Area (mm²)</td>
<td>0.14</td>
<td>0.22</td>
<td>0.2</td>
<td>0.38</td>
<td>0.13</td>
</tr>
</tbody>
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Conclusion

- PD with MDCC
  - PD with Half-Transparent (HT) architecture is sensitive to duty cycle.
  - This project uses a modified DCC to solve the problem of duty-cycle sensitivity.
  - The modified DCC can also solve the problem of stuck locking.

- A multiphase DLL
  - There are 12-phase outputs.

- Frequency Multiplier (FM)
  - This project realizes a 12 times frequency multiplier (Maximum frequency output 3GHz).
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Thank you and Q & A