16-channel readout ASIC for a hodoscope

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Introduction

- **Application:** Hadron therapy
- **Project:** Time-of-Flight Compton Camera for real time visualisation of the nuclear treatment
- **Hodoscope:** X,Y position of the beam, time tagging
  - 128 channel X, 128 channel Y
  - scintillating fibers coupled to photomultiplier tubes (PMT)

![Diagram of a hadron therapy setup with a carbon beam and a patient, showing the hodoscope setup with scintillating fibers and photomultiplier tubes.]

Scintillating fibers hodoscope
First prototype
Introduction

Specifications of readout ASIC

**Detector:** Scintillating fibers +PMT
- Detector Capacitance = 35pF
- Signal rise time  4ns
- Signal fall time  16ns
- Input charge  2pC ~ 10pC
- Counting rate of the whole detector: $10^8$ pps for $^{12}$C ions (10ns)

**ASIC:**
- Bandwidth $\geq$ 87.5Mhz
- Input signal range  200$\mu$A ~ 1mA
- Equivalent Noise Charge $\leq$ 200fC
- 4-bit adjustable gain [2, 1, 0.5, 0.25]: compensate detector’s dispersion
- Dead time of each channel $\leq$ 10ns

→ **Choice of technology:** AMS SiGe BiCMOS 350nm Process
Current conveyor: Low input impedance, Adjustable gain (Easy implementation), High impedance current output
Current comparator: High sensitivity, Small dead time
Charge sensitive amplifier: Only in the test for verifying quantity of input charge
Super Common-Base Input stage (using high-\(g_m\) BJT components): High speed, Very low input impedance

\[
Z_{in} = \frac{1}{(1+A_0)*(g_{m1}+sC_{pi})}
\]

with \(A_0 = g_{m2} * R_{C,SCB}\)
Current Conveyor

- Current Mirror Group: 4-bit adjustable gain controlled by switch

\[
\frac{I_{\text{out}}}{I_{\text{in}}} = \frac{g_{m,\text{MP2-MP5}}}{g_{m,\text{MP1}}} \cdot \frac{1}{\left(1 + s \frac{C_1}{g_{m,\text{Q1}}}ight) \cdot \left(1 + s \frac{C_2}{g_{m,\text{MP2-MP5}}}ight)}
\]

\[C_1 = C_{\text{be1}} \text{ and } C_2 = \sum C_{\text{nodeG}}\]

\[C_2 >> C_1, \quad g_{m,\text{Q1}} >> g_{m,\text{MP2-MP5}}\]

the bandwidth is limited by \(g_{m,\text{MP2-MP5}}\) and \(C_2\)
Current comparator

- Block diagram
  - Input stage
  - Buffered output stage

- Advantages:
  - Dynamic Speed
  - Well adapted to very front-end stage
Current comparator

- Input stage – Current comparison ($I_{out} = I_{sig} - I_{th}$)
Current comparator

• Output stage - Current-to-Voltage Conversion with buffered output

\[ I_{out} = 0 \text{ when } I_{sig} \leq I_{th} \Rightarrow Q1,Q2 \text{ cut off, Voltage at node } D \Rightarrow V_{cc} \]

\[ I_{out} = I_{sig} - I_{th} \text{ when } I_{sig} > I_{th} \Rightarrow Q1,Q2 \text{ conductive, Voltage at node } D \Rightarrow GND \]
Charge Sensitive Amplifier

- Integrator based on folded-cascode amplifier
- $V_{\text{out\_CSA}} = -Z_f \int I_{\text{in}} \, dt$ where $Z_f = R_f \parallel C_f$
- DC Gain = 62dB, Phase margin = 82 deg

PMOS input transistor

Bipolar cascode transistor

Add a zero for stability
Testing and results

Chip and Test board

DUT

S = 6.16 mm²

2.8 mm

2.2 mm
Testing and results

Current conveyor

Current comparator

Charge sensitive amplifier

1 full channel

Indepedant element
Testing and results

Current conveyor

- $I_{in} = C_{inj} \cdot V_{step}/T_{rise}$ with $T_{rise} = 20$ ns
- $ENC = 90 \text{fC}$
- $Z_{in} = V_{in}/I_{in} \approx 24 \Omega$

$C_{inj} = 10 \text{pF}$

$V_{step} = 5 \text{V} \rightarrow 30 \text{mV}$

$I_{in} = 2.5 \text{mA}$

$V_{out} = 10 \text{V} \rightarrow 30 \text{mV}$

$I_{in} = 5 \text{mA}$

$V_{out} = 5 \text{V} \rightarrow 20 \text{mV}$

$V_{in} = 5 \text{V} \rightarrow 20 \text{mV}$
Testing and results

Current comparator
- Offset = 54 \mu A
- Input dynamic 1mA
Testing and results

- Charge Sensitive Amplifier:
  - Linear Dynamic: 100fC \sim 10pC
  - Conversion gain = 97.8mV/pC
  - Equivalent Noise Charge (Cd = 1pF): \sim 113fC

\[
Q_{in} = C_{inj} \cdot V_{step}
\]
### Testing and results

<table>
<thead>
<tr>
<th></th>
<th>INL</th>
<th>ENC</th>
<th>Peaking time</th>
<th>Rise time</th>
<th>Fall time</th>
</tr>
</thead>
<tbody>
<tr>
<td>CC</td>
<td>6%@Qin&lt;0.5pC +/- 2%@Qin&gt;0.5pC</td>
<td>90 fC</td>
<td>___</td>
<td>2 ns</td>
<td>2 ns</td>
</tr>
<tr>
<td>CSA</td>
<td>4%@Qin&lt;0.5pC +/- 1%@Qin&gt;0.5pC</td>
<td>10 fC</td>
<td>28 ns</td>
<td>___</td>
<td>2.3 µs</td>
</tr>
</tbody>
</table>

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<thead>
<tr>
<th></th>
<th>Offset</th>
<th>Propagation time</th>
</tr>
</thead>
<tbody>
<tr>
<td>Current Comparator</td>
<td>54 µA</td>
<td>10 ns</td>
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</table>

<table>
<thead>
<tr>
<th></th>
<th>INL (CC+CSA)</th>
<th>ENC (CC+CSA)</th>
<th>Power consumption (CC+CSA +Comp)</th>
<th>Conversion Gain (CSA)</th>
<th>Xtalk</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 full channel</td>
<td>8%@Qin&lt;1pC 4%@Qin&gt;1pC</td>
<td>90.5 fC</td>
<td>15.8 mW (gain 0.25)</td>
<td>95 mV/pC</td>
<td>1.7%</td>
</tr>
</tbody>
</table>
Conclusion

• 1. This ASIC is adapted to the application
• 2. In next version:
  Time stamp block
  Slow Control (I2C)
• 3. 64 channels in the next chip (4 ASIC/hodoscope)
• Thank you for your attention